



DIC112

(DI32-5)
MicroPC Isolated
Digital/Frequency Input Card

User Manual

Rev. 001 E
March 2009

P R E L I M I N A R Y

Product Title: DIC112
Document name: DIC112 User Manual
Manual version: 001 E
Ref. doc. v.: 03.09 R (DI32-5_UM)

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Revision Record

Rev. Index	Brief Description of Changes	Board Index	Date of Issue
000	Initial version	DIC112	March 2009
001	Mistakes corrected, appendix added	DIC112	March 2009

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Notation Conventions



Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.



Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!



Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product.



Warning!

Information marked by this symbol is essential for human and equipment safety. Read this information attentively, be watchful.



Note...

This symbol and title marks important information to be read attentively for your own benefit.

General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Warning!

When handling this product, special care must be taken not to hit the heatsink (if installed) against another rigid object. Also, be careful not to drop the product, since this may cause damage to the heatsink, CPU or other sensitive components as well.

Please, keep in mind that any physical damage to this product is not covered under warranty.



Note:

This product is guaranteed to operate within the published temperature ranges and relevant conditions. However, prolonged operation near the maximum temperature is not recommended by Fastwel or by electronic chip manufacturers due to thermal stress related failure mechanisms. These mechanisms are common to all silicon devices, they can reduce the MTBF of the product by increasing the failure probability. Prolonged operation at the lower limits of the temperature ranges has no limitations.



Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that your mains power is switched off.

Always disconnect external power supply cables during all handling and maintenance operations with this module to avoid serious danger of electrical shock.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your system. Keep in mind the following:



ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by human being static discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling operations and inspections of this product must be performed with due care, in order to keep product integrity and operability:

- Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.
- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause short-circuit and result in damage to the battery and other components.
- Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably by the front panel, card edges or ejector handles. Avoid touching the components and connectors.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. **DO NOT** apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated fully in their sockets.

Handling

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

In order to keep Fastwel's warranty, you must not change or modify this product in any way, other than specifically approved by Faswel or described in this manual.

Technical characteristics of the systems in which this product is installed, such as operating temperature ranges and power supply parameters, should conform to the requirements stated by this document.

Retain all the original packaging, you will need it to pack the product for shipping in warranty cases or for safe storage. Please, pack the product for transportation in the way it was packed by the supplier.

When handling the product, please, remember that the module, its components and connectors require delicate care. Always keep in mind the ESD sensitivity of the product.

Three Year Warranty

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period for Fastwel products is 36 months since the date of purchase.

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
2. Products, which have been subject to power supply reversal, misuse, neglect, accident, improper installation or storage.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Brief Description

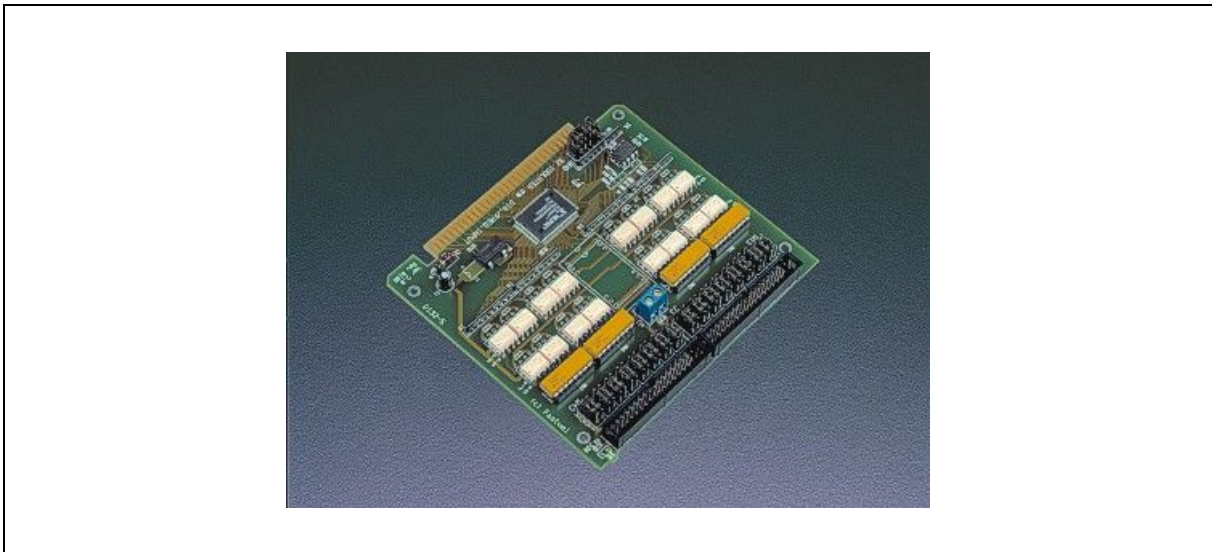
1.1 Module Introduction

The DIC112 (DI32-5) card is designed in Micro PC format and accepts 32 digital or frequency inputs from 3.2 V to 52 V DC. All lines are isolated from system and from each other.

The module uses an FPGA chip (XILINX XC5204™) for signal processing, which allows changing the operation algorithm with no changes in topology. The input channels can be connected in differential or single-ended (with common ground) modes. The DIC11202 provides dry contact support using the on-board 12V DC/DC converter or external (up to 52V) source.

The processing algorithms (Circuit Codes) description can be found in the appendix to this Manual. By default, the module is supplied with the “D00” Circuit Code enabled.

Figure 1.1: DIC112 Module Appearance



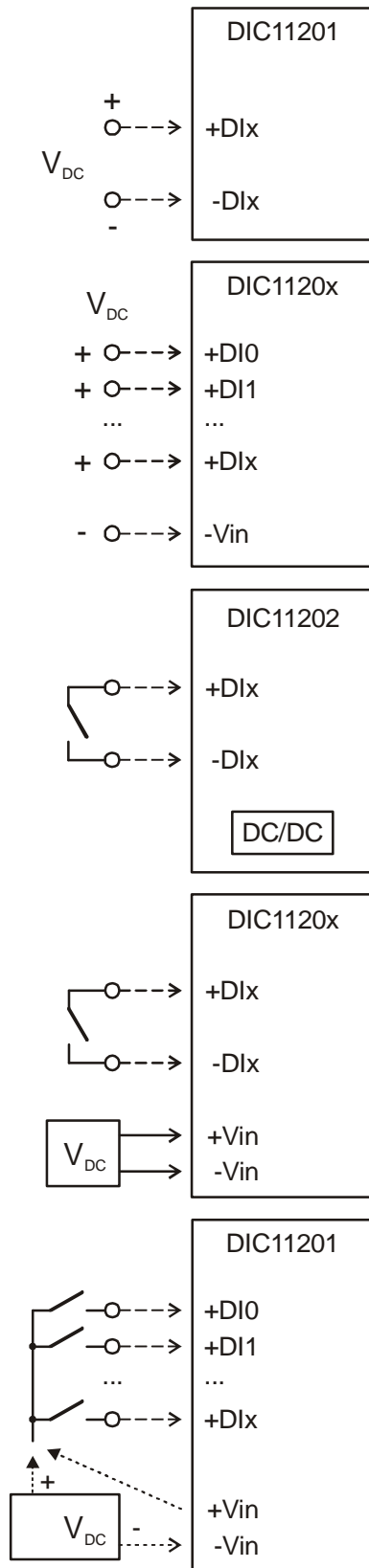
The appearance may vary for different versions of the module.

Main features:

- 32 isolated digital input or frequency measurement channels
- Differential or single-ended connection
- Input voltage range:
DIC11201 – ± 3.2 V to ± 52 V (5 sub-ranges)
DIC11202 – ± 10.2 to ± 25 V
- Input delay: 25 μ s max
- Input current range: 3 to 10 mA
- Input frequency up to 30kHz / 5MHz
- 32-channels frequency measurement
- Programmable debounce logic
- Interrupts generation on input events (\downarrow , \uparrow , \downarrow and \uparrow)
- On-board isolated 12 V DC/DC converter for dry contact support (for DIC11202 only)
- 1500 V isolation to system and between channels
- 5 shared interrupt lines (IRQ3...7)
- 1 shared DMA channel (DRQ1/DACK1)
- Extended operating temperature range from -40°C to $+85^{\circ}\text{C}$

1.2 Signals Connection

The signal lines are connected to the module via J1 and J2 IDC-34 headers. Two TB-34 series terminal boards and two FC34 ribbon cables are used for external connections.



Differential connection

This connection type provides isolation between channels and from the system. Each input signal is connected via a pair of wires (with no common wire) to the contacts +DIx and -DIx, where $x = 0 \dots 31$.

Single-wire discrete signals connection

This connection type is used when signals have a common wire (ground or other potential), and input signals are isolated only from system. Each signal is connected to an appropriate +DIx contact, where $x = 0 \dots 31$, and the common wire - to one of the -Vin contacts of J1, J2, or J3 connectors.

Two-wire dry contacts connection

For this connection type the dry contact is connected to +DIx and -DIx contacts, where $x = 0 \dots 31$.

The internal isolated +12 V power supply or an external (V_{DC}) power supply connected to +Vin and -Vin contacts of J3 connector are used as a power source for dry contacts.

Single-wire dry contacts connection

For this connection type the signal is connected to the appropriate +DIx contact, where $x = 0 \dots 31$, and the common wire is connected to +Vin contact of the J3 connector, when the internal power supply is used. When an external power supply is used, the common wire is connected to "+" of the power supply, and its "-" is connected to -Vin contact of any of J1, J2, or J3 connectors.

**Attention!**

Changing of the connection type requires appropriate setting of W12 ... W43 jumpers!

2 Installation

The module can be installed in MicroPC card cages, in IBM PC ISA slots, or can be connected to other modules using a flexible cable.



ESD Sensitive Device!

The module contains components sensitive to static electricity. Installation or removal of the module, cables connection while the power is on can damage the module.



Attention!

When installing the module in a 62-contact ISA connector it is necessary to observe correct orientation of the module. Incorrect orientation (with 180° rotation) leads to serious damage to the module!



Attention!

Before switching the module on, make sure that jumpers BA[5:0] and W[43:12] are set correctly!

1.3 Base Address Setting

The jumpers BA[5:0] allow setting the module's Base Address or the input-output area address segment, in which the module will be accessible by the system. The module is accessed, when SA[9:4] address bits match BA[5:0]; the Access Indicator is lit.

Base Address (Hex)	BA5	BA4	BA3	BA2	BA1	BA0
000h	0	0	0	0	0	0
010h	0	0	0	0	0	1
...
100h	0	1	0	0	0	0
110h(*)	0	1	0	0	0	1
...
200h	1	0	0	0	0	0
...
3E0h	1	1	1	1	1	0
3F0h	1	1	1	1	1	1

(*) Factory setting; 1 = closed; 0 = open

**Attention!**

Incorrect Base Address setting can lead to system conflicts. Before switching the module on, make sure that the set Base Address is not used in your system.

1.4 Interrupt Lines Setup

The module can use five shared interrupt lines (IRQ3...7). The interrupt line selection is performed by software and depends on the Circuit Code (see Appendix to this Manual). The interrupts are not enabled on power-up.

1.5 Input Signals Type Selection

The W12...W43 Input Type jumpers allow selecting the signal connection type for each channel or for groups of channels.

Input Channel Number	Two-Wire Discrete Input (DIC11201 Factory Setting)	Single-wire Discrete Input and Dry Contact	Two-Wire Dry Contact (DIC11202 Factory Setting)
0	W12[2-3]	W12[3-4]	W12[1-2] & [3-4]
1	W13[2-3]	W13[3-4]	W13[1-2] & [3-4]
...
7	W19[2-3]	W19[3-4]	W19[1-2] & [3-4]
8	W20[2-3]	W20[3-4]	W20[1-2] & [3-4]
...
30	W42[2-3]	W42[3-4]	W42[1-2] & [3-4]
31	W43[2-3]	W43[3-4]	W43[1-2] & [3-4]

**Attention!**

Only indicated contacts should be closed. The rest must be open!

1.6 Input Voltage Range Selection

The module is designed for operation with the input voltage range from 3.2 V to 52 V (5 sub-ranges). Operation threshold for each 8-channel group is set with the help of SIP resistor arrays (RN1, RN2, RN3, RN4) and can be changed by the customer.

Sub-range	Voltage, V	Resistor rating	Note
1	3.2...12	470 Ω	Supplied with DIC11201
2	10.2...25	2.2 k Ω	Initially installed
3	20...35	4.7 k Ω	Supplied with DIC11201
4	29...42	6.8 k Ω	
5	41...52	10 k Ω	Supplied with DIC11201

3 Module Control

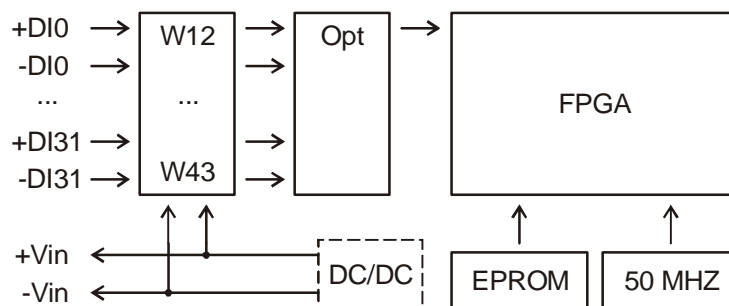
The module is controlled via I/O ports; their designation depends on Circuit Code loaded in FPGA. This chapter describes only standard ports, whose operation does not depend on the loaded Circuit Code. The rest ports are described in the Appendix to this manual related to an appropriate Circuit Code.

3.1 Main Functional Units of the Module

The module contains the following main functional units:

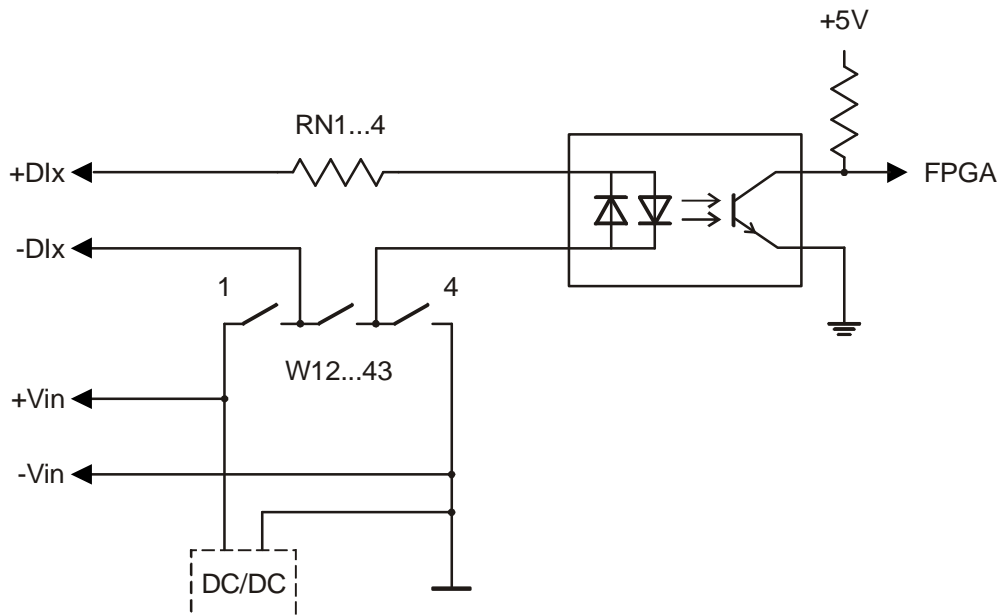
- FPGA
- EPROM
- Opto-isolation unit (Opt)
- Jumpers (W12...W43)

DIC112 functional diagram:



3.2 Input Channel Circuit

The input channel circuit diagram is shown on the picture below. Incoming signal via a limiting resistor comes to an optocoupler. W12...W43 jumpers allow to select the connection type (two-wire, single-wire, dry contact). Output from the optocoupler is routed to FPGA input.



3.3 Interrupts Programming

The shared interrupt line is set via the byte port with BA+13 address ("BA" is the module's Base Address). The port is available for read and write.

Interrupts register:

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA+13	-	-	-	-	-	LN2	LN1	LN0

$LN[2:0]$ Interrupt line code ($LN[2:0] = 3...7$). The interrupt line is enabled by writing the code corresponding to the line IRQ3...IRQ7.

All interrupt lines are disabled on power-up.

3.4 DMA Channel and IOCHRDY Lines

The module can use one shared direct access channel (DRQ1/DACK1) and the IOCHRDY line. The DMA channel and availability signal request method depends on the Circuit Code in use. The method for the particular Circuit Code is described in the Appendix. The DMA channel and IOCHRDY signal are disabled on power-up.

3.5 ID of the Module

The module can be identified by the Circuit Code loaded in FPGA. The ID is read via the byte ports with addresses BA+14, BA+15 ("BA" is the module's Base Address).

Module's ID:

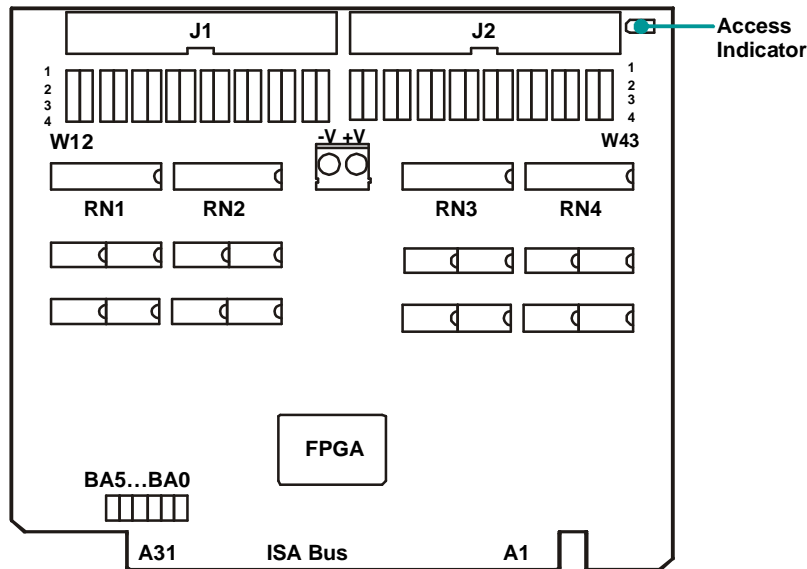
Address	D7	D6	D5	D4	D3	D2	D1	D0
BAx+14	'D'							
BAx+15	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0

'D' ASCII-code of the letter "D";

SN[7:0] The Circuit Code number (SN[7:0] = 0...255).

4 Technical Information

4.1 Components Layout



4.2 Technical Specifications

Power voltage:		5V ± 5%
Consumption current:	DIC11201	260 mA
	DIC11202	400 mA
Input voltage:	DIC11201	± 3.2 to ±52 V
	DIC11202	± 10.2 to ±25 V
Inputs isolation voltage:		1500 V
Operating temperature range:		-40 ...+85°C
Storage temperature:		-55 ...+90°C
Humidity:		up to 95% at +25°C

4.3 Connectors' Pinouts

ISA connector, rows A and B:

#	Signal	Type	#	Signal	Type
A1	IOCHK*	-	B1	0V	In
A2	SD7	In/Out	B2	RESET	In
A3	SD6	In/Out	B3	+5V	In
A4	SD5	In/Out	B4	IRQ9	-
A5	SD4	In/Out	B5	-5V	-
A6	SD3	In/Out	B6	DRQ2	-
A7	SD2	In/Out	B7	-12V	-
A8	SD1	In/Out	B8	0WS*	-
A9	SD0	In/Out	B9	+12V	-
A10	IOCHRDY	Out, 3	B10	AGND	-
A11	AEN	In	B11	SMEMW*	-
A12	SA19	-	B12	SMEMR*	-
A13	SA18	-	B13	IOW*	In
A14	SA17	-	B14	IOR*	In
A15	SA16	-	B15	DACK3*	-
A16	SA15	In	B16	DRQ3	-
A17	SA14	In	B17	DACK1*	In
A18	SA13	In	B18	DRQ1	Out, 3
A19	SA12	In	B19	DACK0*	-
A20	SA11	In	B20	BCLK	-
A21	SA10	In	B21	IRQ7	Out, 3
A22	SA9	In	B22	IRQ6	Out, 3
A23	SA8	In	B23	IRQ5	Out, 3
A24	SA7	In	B24	IRQ4	Out, 3
A25	SA6	In	B25	IRQ3	Out, 3
A26	SA5	In	B26	DACK2*	-
A27	SA4	In	B27	TC	-
A28	SA3	In	B28	BALE	-
A29	SA2	In	B29	+5V	-
A30	SA1	In	B30	OSC	-
A31	SA0	In	B31	0V	In

In the table above: In = Input
 In/Out = Input/Output
 Out, 3 = Output with 3-d state

J1, J2, J3 connectors:

#	J1 Signal	J2 Signal	J3
1	+DI0	+DI16	+Vin
2	-DI0	-DI16	-Vin
3	+DI1	+DI17	
4	-DI1	-DI17	
5	+DI2	+DI18	
6	-DI2	-DI18	
7	+DI3	+DI19	
8	-DI3	-DI19	
9	+DI4	+DI20	
10	-DI4	-DI20	
11	+DI5	+DI21	
12	-DI5	-DI21	
13	+DI6	+DI22	
14	-DI6	-DI22	
15	+DI7	+DI23	
16	-DI7	-DI23	
17	+DI8	+DI24	
18	-DI8	-DI24	
19	+DI9	+DI25	
20	-DI9	-DI25	
21	+DI10	+DI26	
22	-DI10	-DI26	
23	+DI11	+DI27	
24	-DI11	-DI27	
25	+DI12	+DI28	
26	-DI12	-DI28	
27	+DI13	+DI29	
28	-DI13	-DI29	
29	+DI14	+DI30	
30	-DI14	-DI30	
31	+DI15	+DI31	
32	-DI15	-DI31	
33	-Vin	-Vin	
34	-Vin	-Vin	

5 Appendix “D00”

FPGA Circuit Code “D00”: Interrupt generator on events with programmable debounce and 32-channel frequency meter.

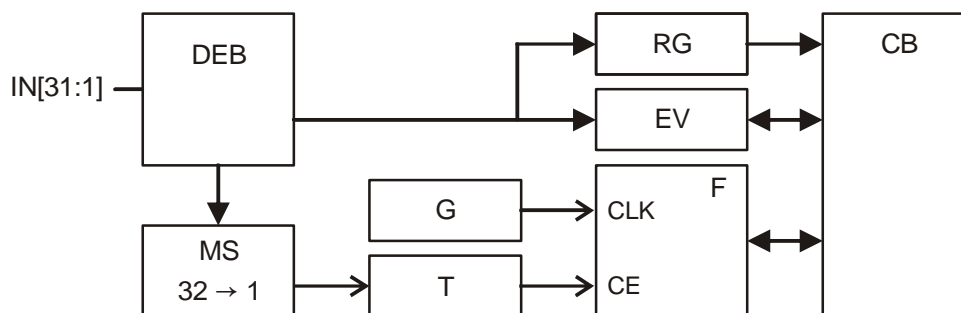
5.1 Features

The D00 FPGA circuit variant enables the following DIC112 features:

- Programmable debounce for each 8-channel group: 40 ns, 400 ns, 4.5 ms, 140 ms
- Programmable event front for each 8-channel group: 1→0, 0→1, (1→0 + 0→1)
- Maskable interrupt generation from each 8-channel group
- 32-channel frequency meter:
 - Method of measurement: filling with reference frequency
 - Programmable reference frequency interval: $(2...256) \times 40$ ns
 - Programmable number or periods of the measured frequency: 1...255
 - Accuracy: up to 16 bit
 - Interrupt generation from the frequency meter

5.2 Functional Units

D00 functional diagram:



FPGA Circuit Code “D00” main functional units:

- ISA bus interface (CB)
- Debounce unit (DEB)
- Inputs register (RG)
- Events registration unit (EV)
- Programmable strobe generator of measured frequency N-periods (T)
- Reference frequency generator (G)
- Frequency measurement counters (F)

5.3 Ports Description

This section presents DIC112 ports designation with BA Base Address for FPGA Circuit Code "D00".

Control register is available for write via the byte ports with addresses BA+0, BA+5, and BA+6 and has the following format:

Control Register:

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA+0	–	–	–	–	–	–	–	<i>BNK</i>
BA+5	<i>CK</i> ₁₃	<i>CK</i> ₀₃	<i>CK</i> ₁₂	<i>CK</i> ₀₂	<i>CK</i> ₁₁	<i>CK</i> ₀₁	<i>CK</i> ₁₀	<i>CK</i> ₀₀
BA+6	<i>FR</i> ₁₃	<i>FR</i> ₀₃	<i>FR</i> ₁₂	<i>FR</i> ₀₂	<i>FR</i> ₁₁	<i>FR</i> ₀₁	<i>FR</i> ₁₀	<i>FR</i> ₀₀

BNK Ports bank (see below);

CK[1:0]_x Debounce time codes for groups of inputs, see tables 1 and 3 below;

FR[1:0]_x Event front codes for groups of inputs, see tables 1 and 2 below

Table 1

Inputs Group (x)	Inputs
0	IN[7:0]
1	IN[15:8]
2	IN[23:16]
3	IN[31:24]

Table 2

FR[1:0]	Event Front for "x" Group of Channels
0	–
1	Rising edge
2	Falling edge
3	Any edge

Table 3

CK[1:0]	Debounce Time for "x" Group of Channels
0	40 ns ± 0.002 %
1	400 ns ± 0.002 %
2	4.5 ms ± 30 %
3	140 ms ± 30 %

Shared interrupt lines are enabled via the available for write byte port with address BA+13:

Interrupt Register:

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA+13	GRP3	GRP2	GRP1	GRP0	INTF	LN2	LN1	LN0

LN[2:0] Interrupt line code ($LN[2:0] = 3...7$). The interrupt line is enabled by writing the code corresponding to the line number: IRQ3...IRQ7;

INTF Enables interrupt from the frequency meter if the bit is set.
Interrupt from the frequency meter – inverted *ST_RDY*;

GRP[3:0] Setting these bits enables interrupts from the input groups IN[31:24], IN[23:16], IN[15:8], IN[7:0] accordingly. The interrupt signal is reset only on clearing of the corresponding bits in the Events Register.

Clearing the bits disables interrupt generation.

The Inputs register is available for read via the word ports with addresses BA+1, BA+3, when *BNK* bit is cleared:

Inputs Register:

Address	BNK	D15	D14	D13	...	D3	D2	D1	D0
BA+1	0	ST15	ST14	ST13	...	ST3	ST2	ST1	ST0
BA+3	0	ST31	ST30	ST29	...	ST19	ST18	ST17	ST16

ST[31:0] Inputs status bits reflect the state of corresponding input (IN31...IN0) with the debounce time delay.

The Events register is available for write and read via the word ports with addresses BA+1, BA+3, when *BNK* bit is set:

Events Register:

Address	BNK	D15	D14	D13	...	D3	D2	D1	D0
BA+1	1	EV15	EV14	EV13	...	EV3	EV2	EV1	EV0
BA+3	1	EV31	EV30	EV29	...	EV19	EV18	EV17	EV16

EV[31:0] Events register bits are set on the change of the corresponding input IN[31:0] status. The event front is defined by *FR[1:0]_x* bits.

Note: Only one event record is stored for each input. To record the next event it is necessary to clear the appropriate event register bit **by writing “1”** in it.

Frequency Meter

The frequency meter has two registers: Control register and Data register. The Control register is available via the byte ports with addresses BA+7, BA+8, and BA+9:

Control Register:

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA+7	<i>ST_RDY</i>	<i>ERR</i>	–	<i>CH4</i>	<i>CH3</i>	<i>CH2</i>	<i>CH1</i>	<i>CH0</i>
BA+8	<i>T7</i>	<i>T6</i>	<i>T5</i>	<i>T4</i>	<i>T3</i>	<i>T2</i>	<i>T1</i>	<i>T0</i>
BA+9	<i>G7</i>	<i>G6</i>	<i>G5</i>	<i>G4</i>	<i>G3</i>	<i>G2</i>	<i>G1</i>	<i>G0</i>

CH[4:0] The code of the input (0...31) connected to the frequency meter.

ERR Measurement error. This bit is set when the frequency meter is overfilled ($F[15:0] > 0xFFFF$). The bit is cleared on any write operation to BA+7 port.

ST_RDY Start/Ready bit. Setting this bit starts frequency measurement; clearing it – stops. The data register status is not defined. This bit is automatically cleared on a successful measurement – when N periods of the measured frequency are received beginning from the back front – or if the meter is overfilled. Reading this bit allows to determine the meter's readiness for the next measurement: “1” = ready, “0” = busy.

T[7:0] The number of measured frequency periods code (1 through 255, the code $T[7:0] = 0$ is not used).

Note: The number of periods code is not saved after the measuring operation is completed. It must be defined before each measurement.

G[7:0] The code of reference frequency (1 through 255, the code $G[7:0] = 0$ is not used). The reference frequency (F) in MHz is calculated using the following equation:

$$F = 25 / (G[7:0] + 1)$$

For example, to specify the reference frequency of 1 MHz, set the code $G[7:0] = 24$.

The 16-bit frequency meter Data register is available for read via the word port with address BA+10:

Data Register:

Address	D7	D6	D5	D4	D3	D2	D1	D0
BA+10	<i>F15</i>	<i>F14</i>	<i>F13</i>	...	<i>F3</i>	<i>F2</i>	<i>F1</i>	<i>F0</i>

F[15:0] The 16-bit code of duration of N periods of the measured frequency. The number of periods is set via $T[7:0]$. Least significant digit corresponds to one reference interval defined by word $G[7:0]$ amounting to 80 ns to 10.24 ms